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*Dipartimento di Ingegneria dell'Informazione,
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**Graphene for nanoelectronic device applications**

**Abstract**

In the past decade, the state of the art Si-based electronics has gone from devices at or above 100 nm to the realm of 30 nm and below, with a defined pathway to devices, logic and memory, of about 15 nm. In addition, as devices have scaled below a gate length of about 100nm performance per power density has not scaled, in fact it has decreased. In order to address the power issues the industry is facing as CMOS devices are scaled further, a program, Nanoelectronic Research Initiative, was created to develop new materials and devices that take advantage of new state variables with the objective of improving performance per power density. Graphene, a mono-layer of carbon atoms arranged in a honeycomb lattice, has recently been subject of considerable theoretical and experimental interest because of its unique transport properties together with exceptional chemical and physical properties. New devices such as BiSFET, TFETs, and P-N junction devices have been proposed and are being evaluated for the next switch. In order to demonstrate any of these new devices, high quality graphene films will have to be developed and integrated with dielectrics and metal contacts.

High quality graphene can be formed by exfoliation from natural graphite with samples sizes of a few hundred square microns. Graphene can also be grown on SiC substrates by a Si evaporation process from either the Si or C surfaces, but these films are limited to SiC and are difficult to integrate on Si wafers. The successful demonstration and implementation of graphene-based device technology will require synthesis of high quality graphene large are films on substrates other than SiC or the exfoliation of graphene from graphite. The discovery of large-area and monolayer graphene growth on Cu substrates has opened many opportunities for the development of graphene-based devices including transparent conductive electrodes. Growth of graphene on Cu by chemical vapor deposition is unlike growth on other substrates such as Ni or Co in that a self-limited monolayer of graphite is grown by a surface limited process. In order to take full advantage of the fundamental properties of graphene it is necessary to grow uniform and nearly defect-free films as the semiconductor industry has done with silicon substrates. Further, integration of this chemically inert material with dielectrics and metals will be necessary in order to demonstrate any electronic device. In this presentation I will review the need for devices beyond CMOS, growth of large area polycrystalline and single crystal graphene, and integration of dielectrics and metals on graphene and their effects on electrical properties of simple FET devices.